FIG. 1

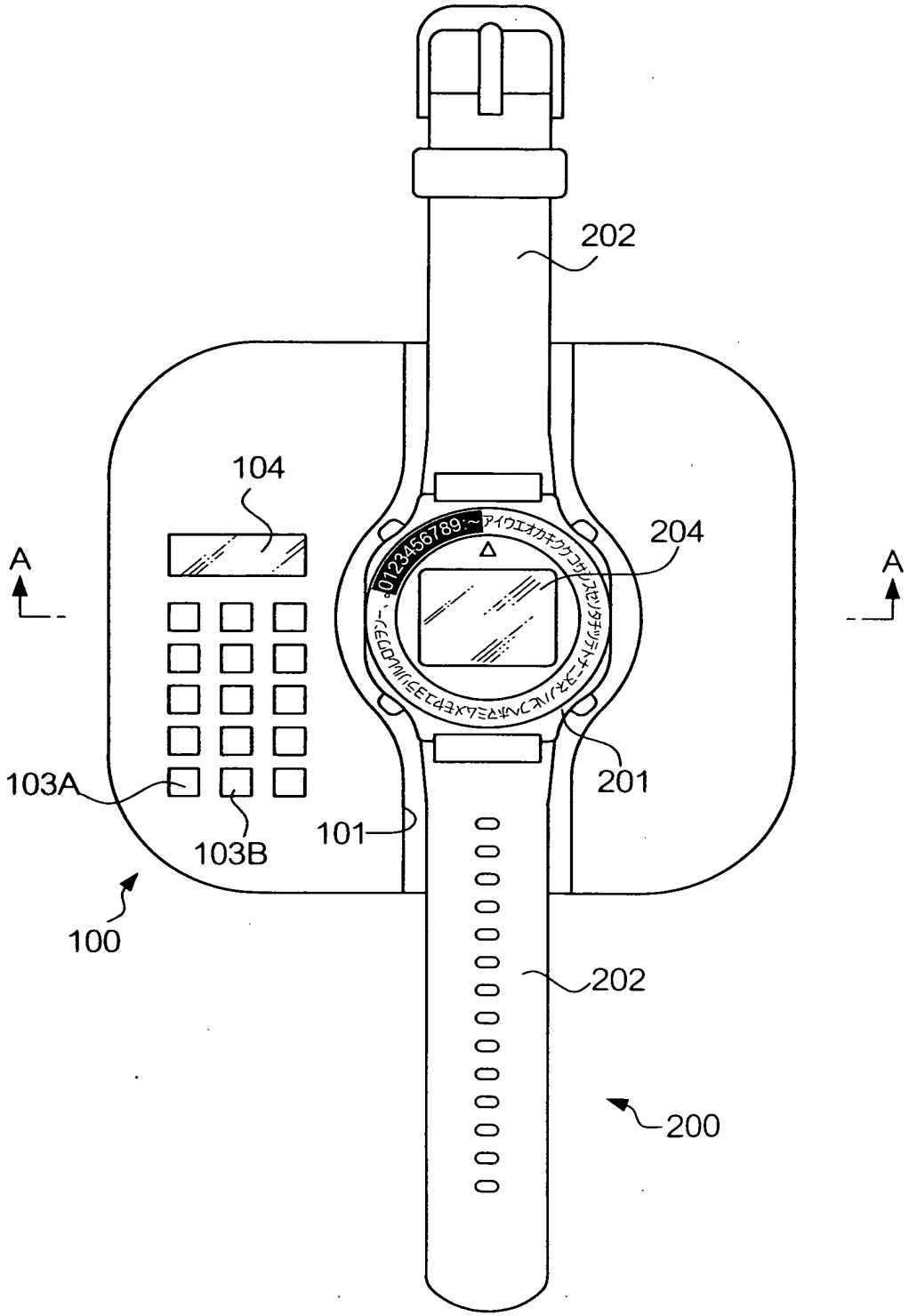


FIG. 2

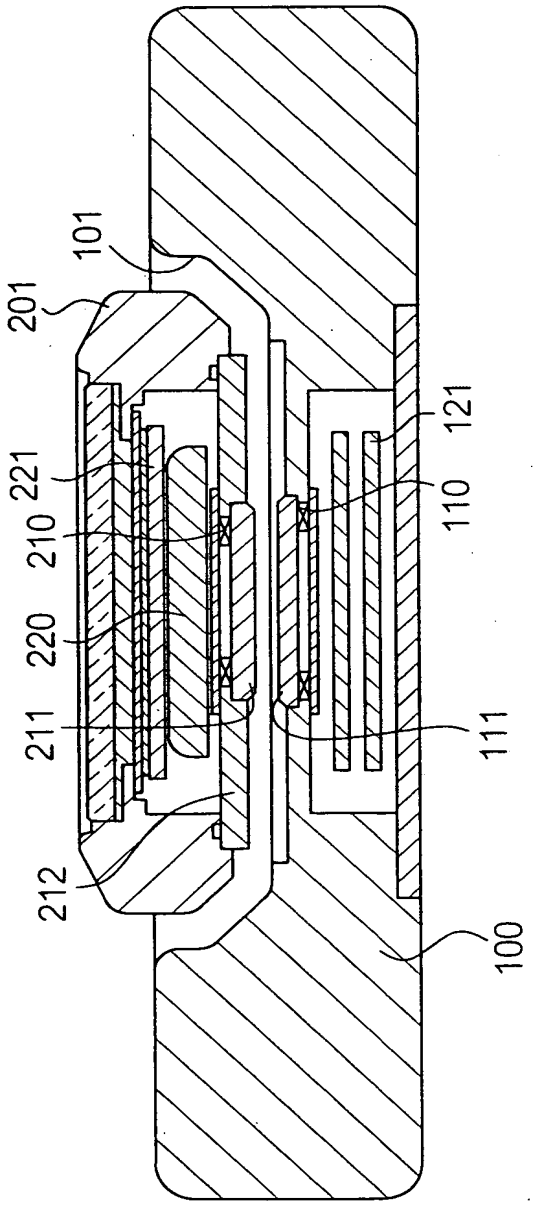


FIG. 3

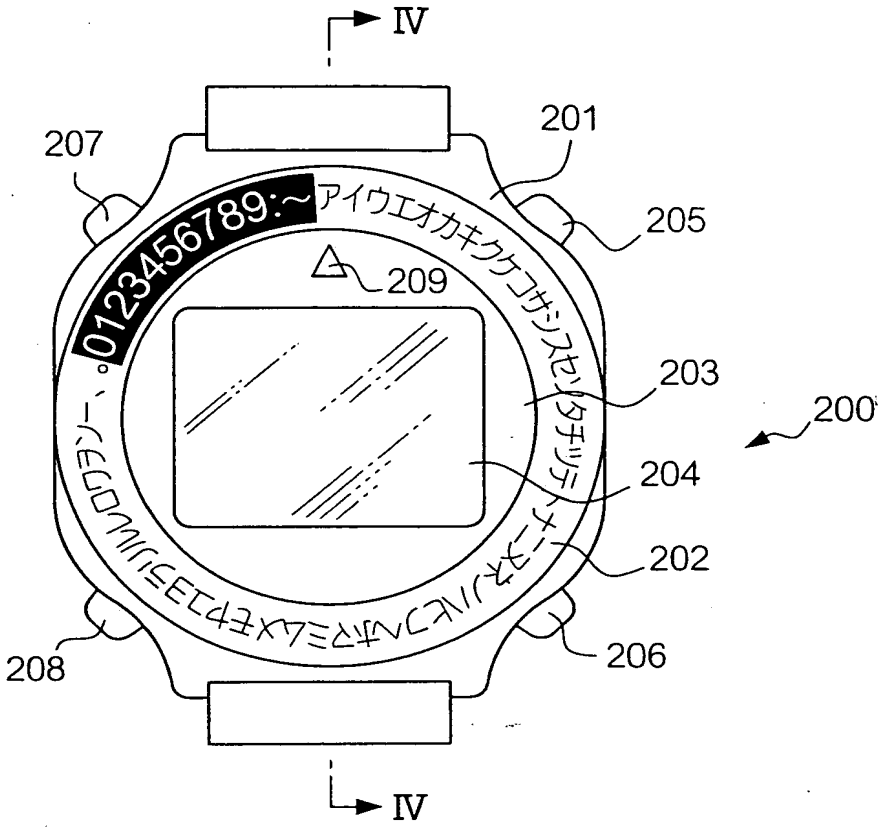

Ⅳ
201
207
205
209
203
200
204
202
208
206
Ⅳ

FIG. 4

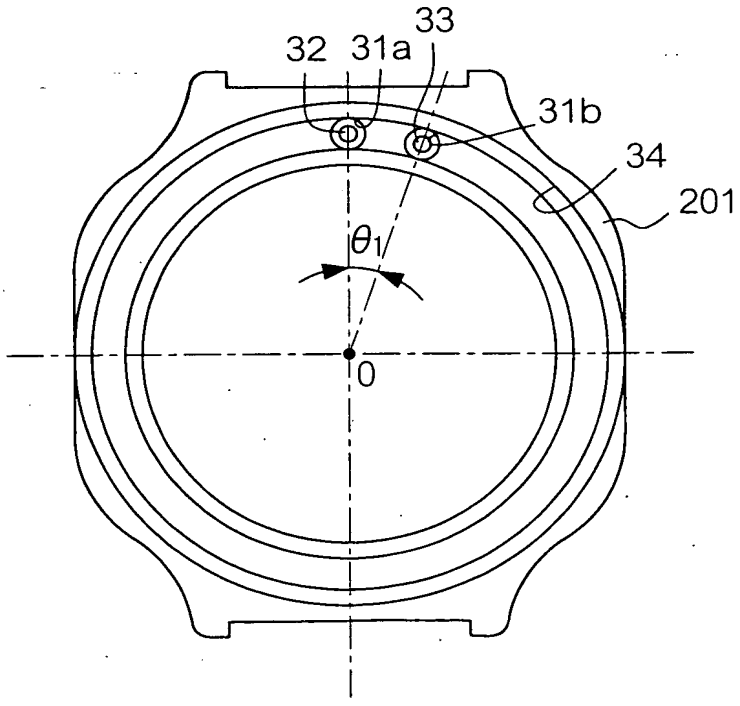

33
32
31a
31b
34
201
θ1
0

FIG. 5

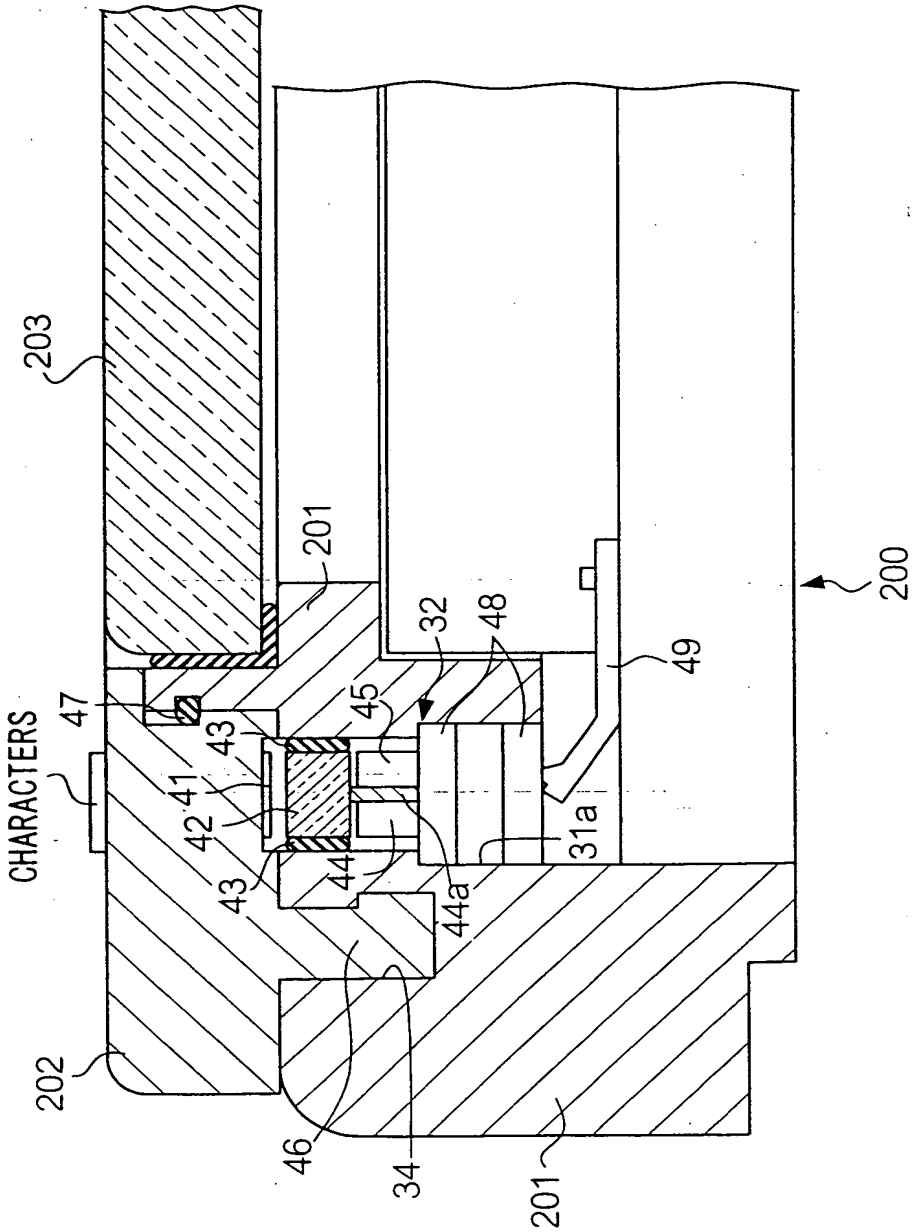

203
201
200
32
48
49
47
45
43
41
42
CHARACTERS
43
44
44a
31a
202
46
34
201

FIG. 6

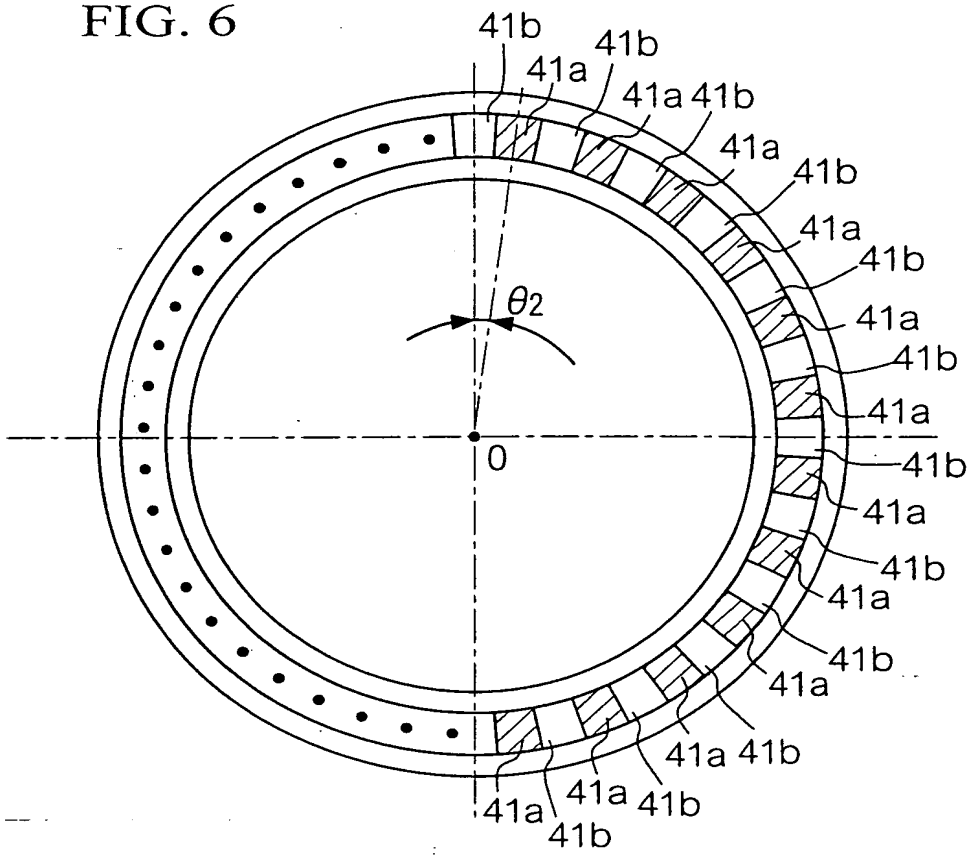


FIG. 7A

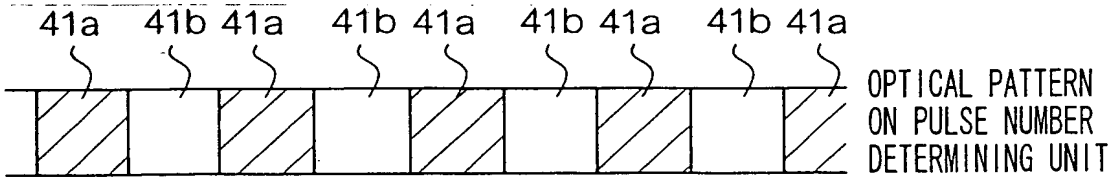


FIG. 7B

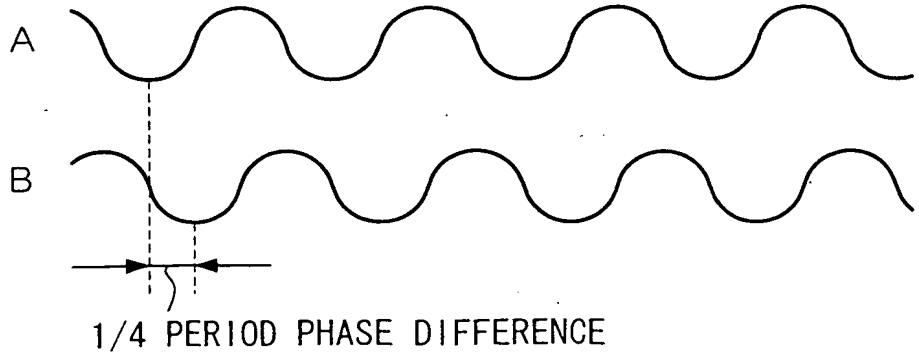


FIG. 8

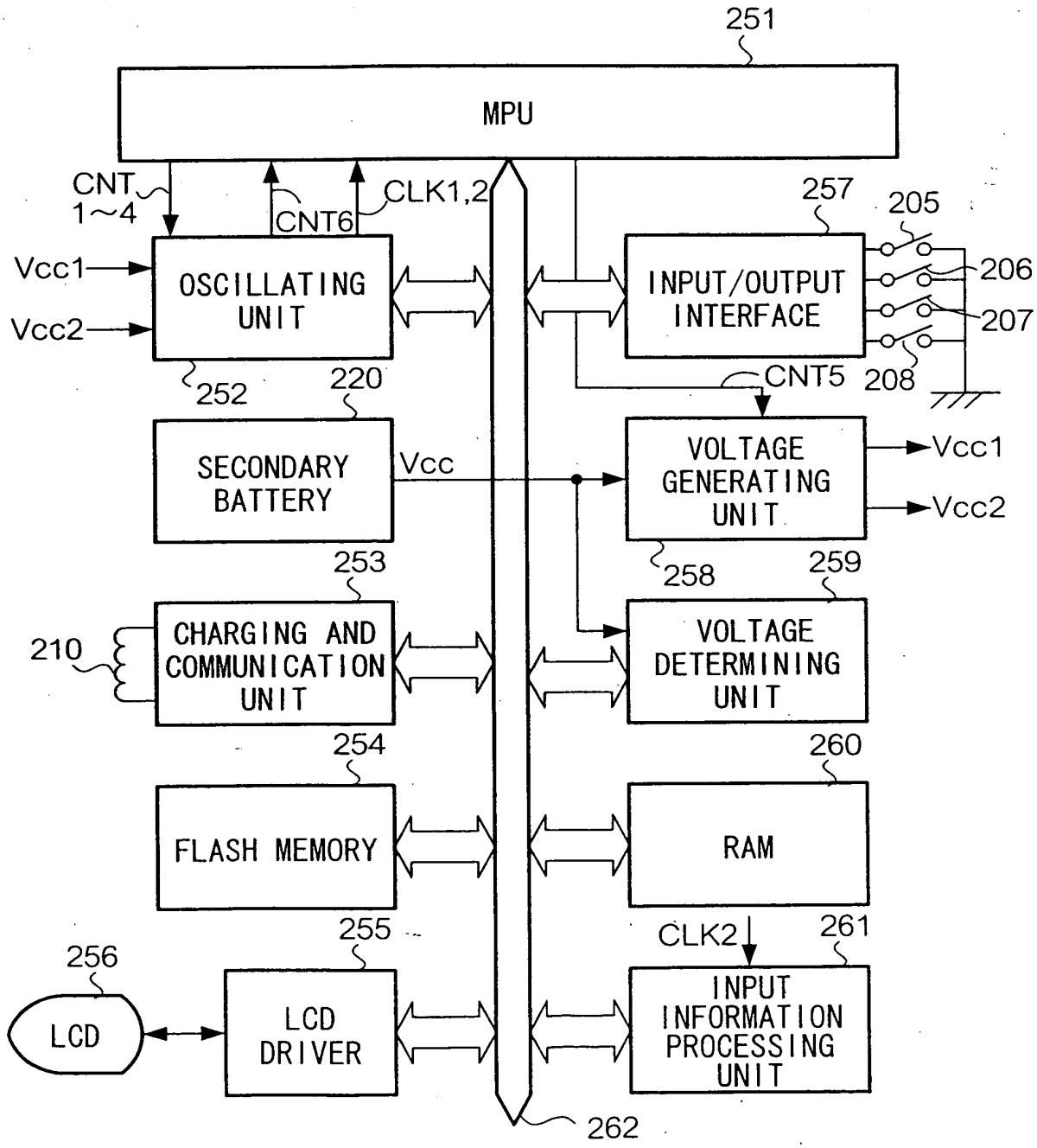

251
MPU
CNT 1~4
CNT6
CLK1,2
257
205
206
207
208
Vcc1
Vcc2
OSCILLATING UNIT
INPUT/OUTPUT INTERFACE
252
220
CNT5
SECONDARY BATTERY
Vcc
VOLTAGE GENERATING UNIT
Vcc1
Vcc2
253
258
259
210
CHARGING AND COMMUNICATION UNIT
VOLTAGE DETERMINING UNIT
254
260
FLASH MEMORY
RAM
255
CLK2
261
256
LCD
LCD DRIVER
INPUT INFORMATION PROCESSING UNIT
262

FIG. 9

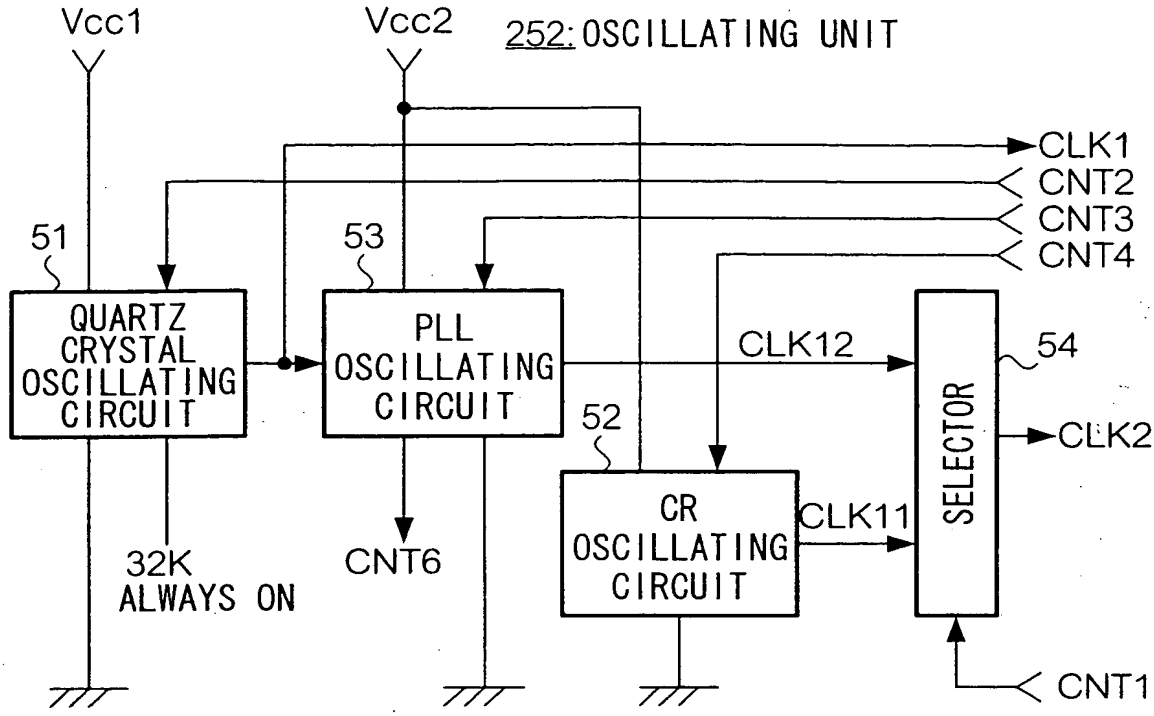

Vcc1
Vcc2
252: OSCILLATING UNIT
CLK1
CNT2
CNT3
CNT4
51
53
QUARTZ CRYSTAL OSCILLATING CIRCUIT
PLL OSCILLATING CIRCUIT
CLK12
54
52
SELECTOR
CLK2
CR OSCILLATING CIRCUIT
CLK11
32K ALWAYS ON
CNT6
CNT1

FIG. 12

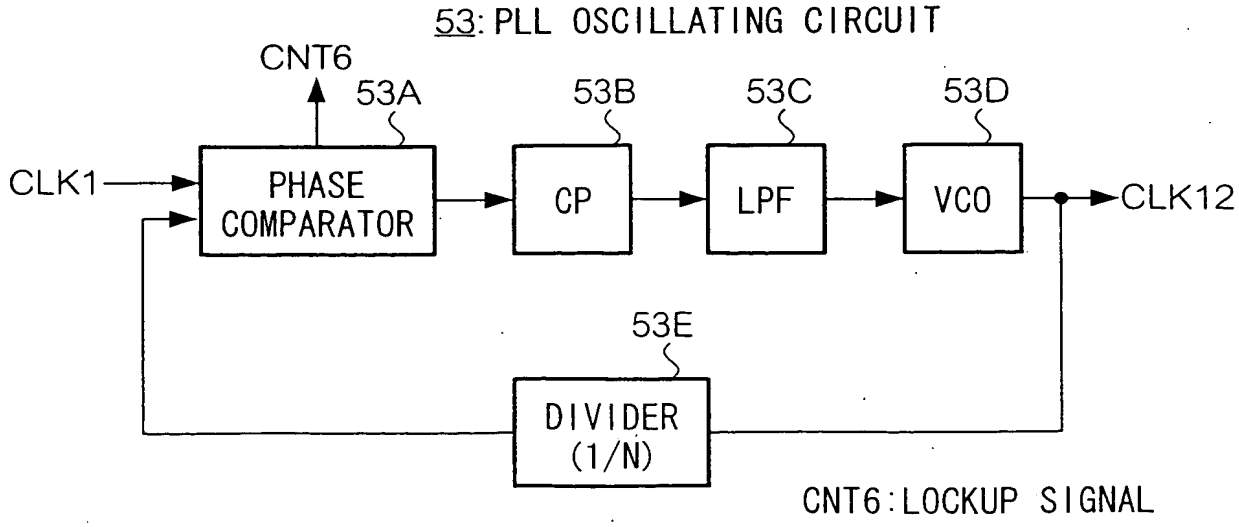

53: PLL OSCILLATING CIRCUIT
CNT6
53A
53B
53C
53D
CLK1
PHASE COMPARATOR
CP
LPF
VCO
CLK12
53E
DIVIDER (1/N)
CNT6: LOCKUP SIGNAL

FIG. 10

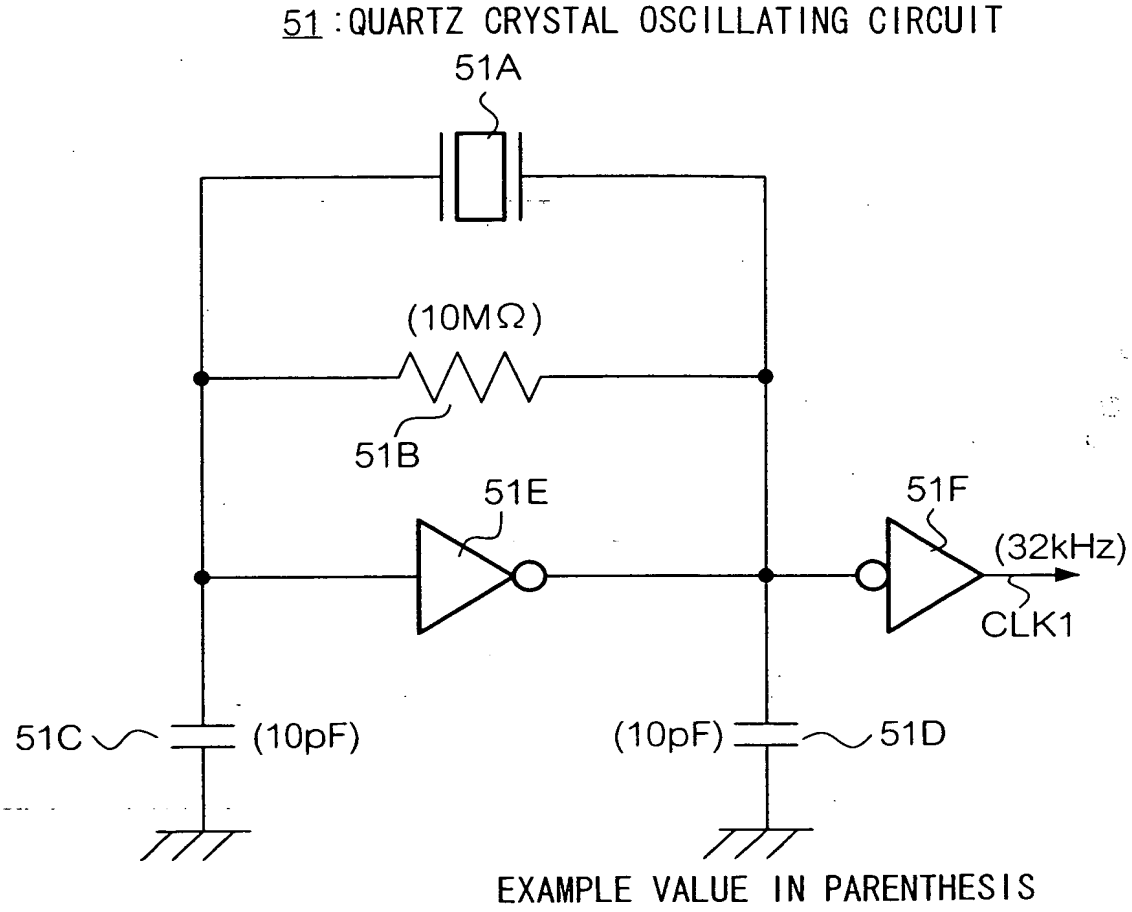

51 : QUARTZ CRYSTAL OSCILLATING CIRCUIT
51A
(10MΩ)
51B
51E
51F
(32kHz)
CLK1
51C
(10pF)
(10pF)
51D
EXAMPLE VALUE IN PARENTHESIS

FIG. 11

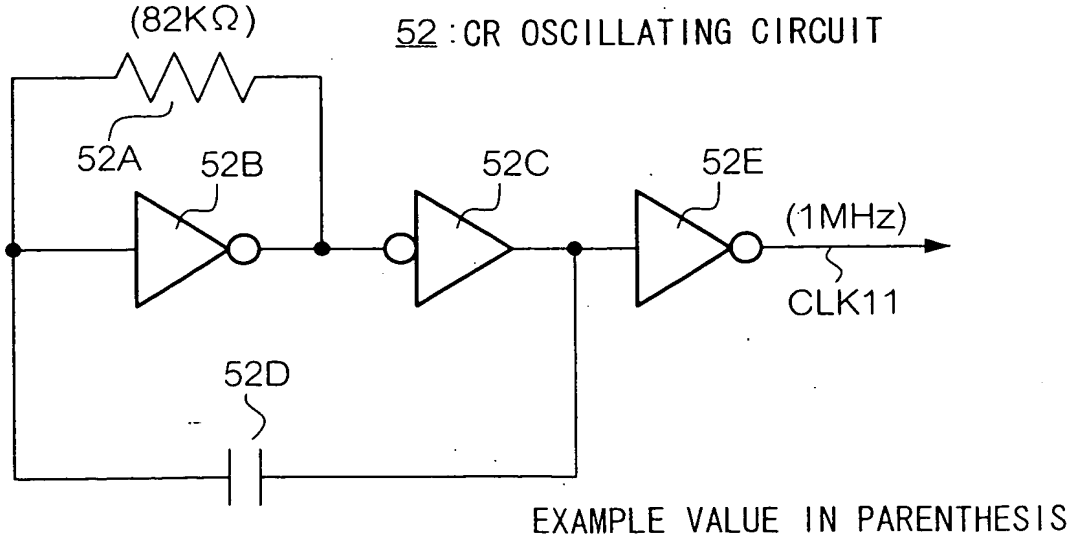

(82KΩ)
52 : CR OSCILLATING CIRCUIT
52A
52B
52C
52E
(1MHz)
CLK11
52D
EXAMPLE VALUE IN PARENTHESIS

FIG. 13

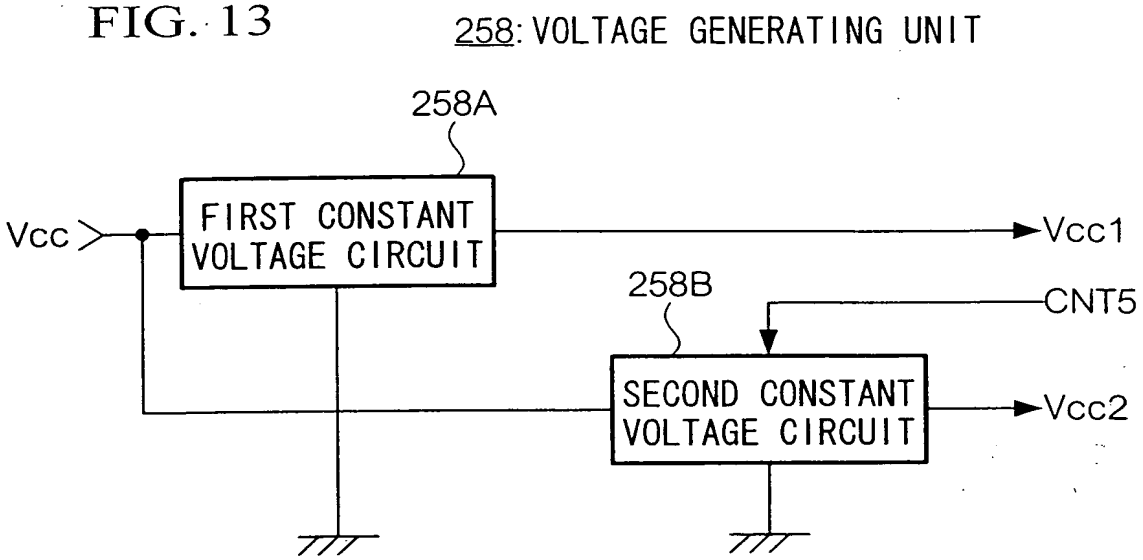

258: VOLTAGE GENERATING UNIT
258A
FIRST CONSTANT VOLTAGE CIRCUIT
Vcc
Vcc1
258B
CNT5
SECOND CONSTANT VOLTAGE CIRCUIT
Vcc2

FIG. 19

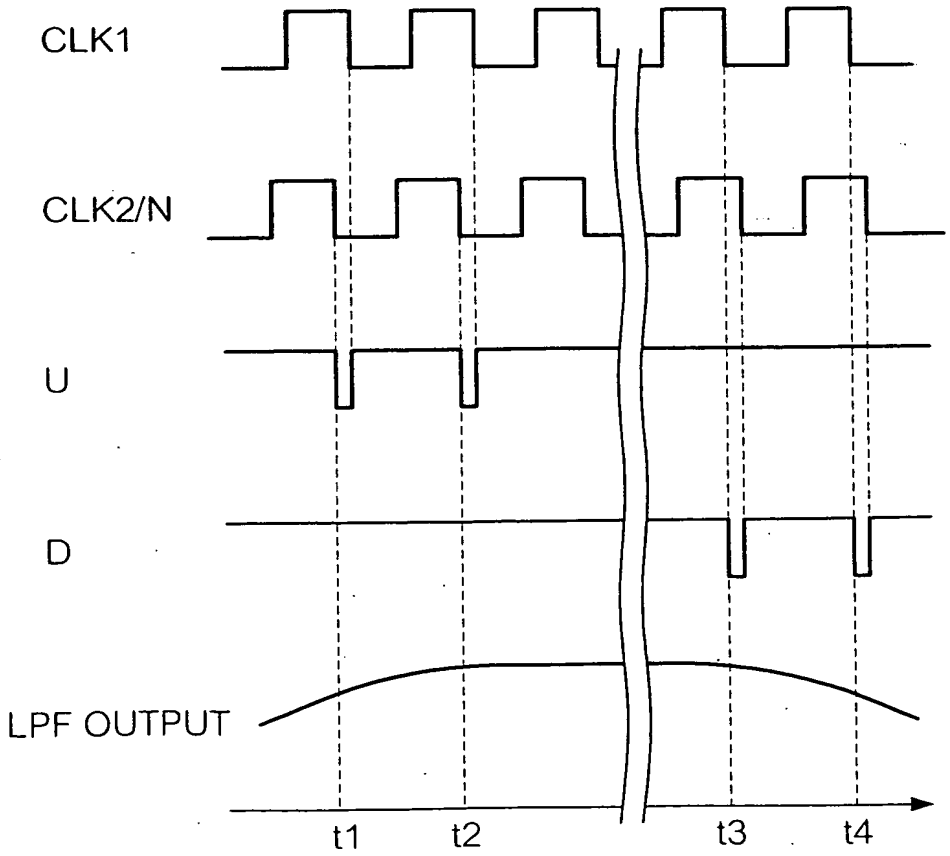
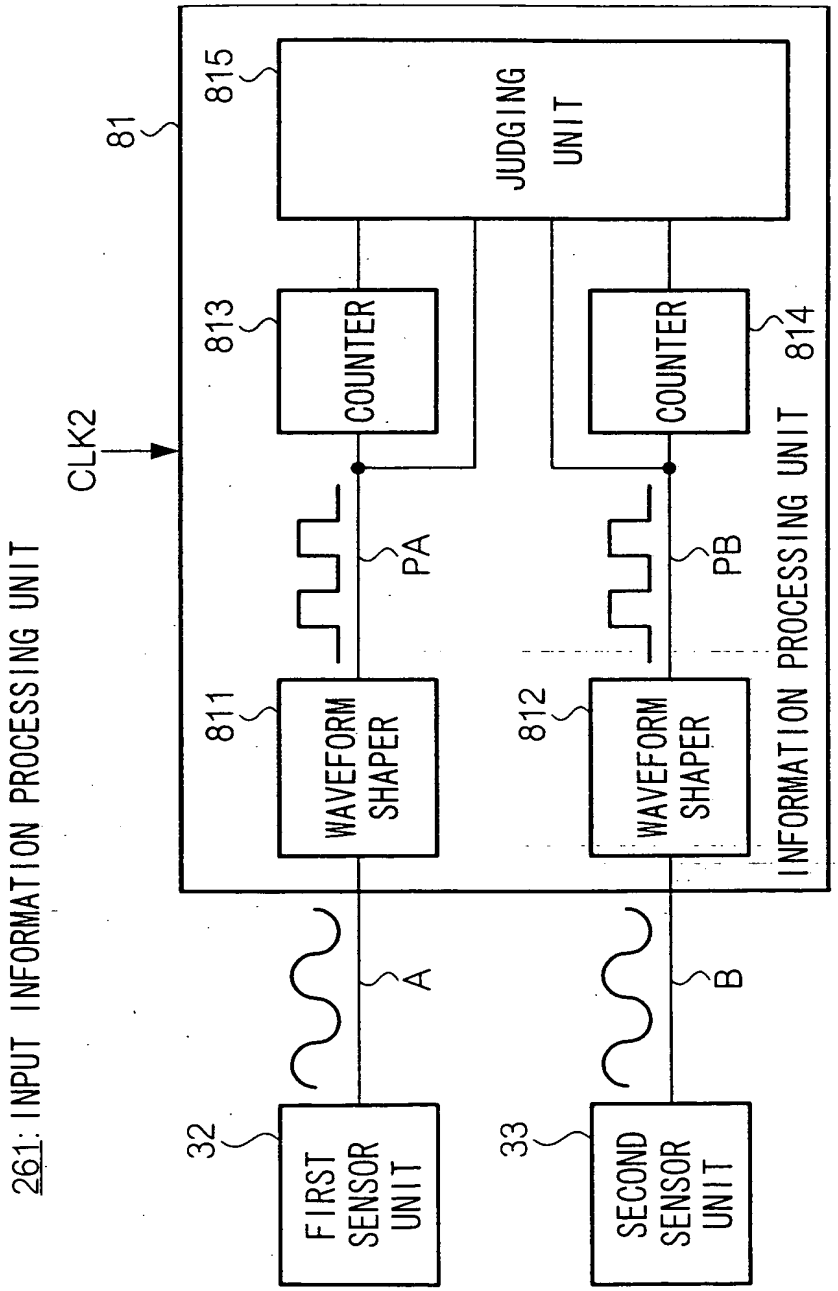

CLK1
CLK2/N
U
D
LPF OUTPUT
t1
t2
t3
t4

FIG. 14


261: INPUT INFORMATION PROCESSING UNIT
CLK2
81
INFORMATION PROCESSING UNIT
815
JUDGING UNIT
813
COUNTER
814
COUNTER
811
WAVEFORM SHAPER
812
WAVEFORM SHAPER
PA
PB
A
B
32
FIRST SENSOR UNIT
33
SECOND SENSOR UNIT

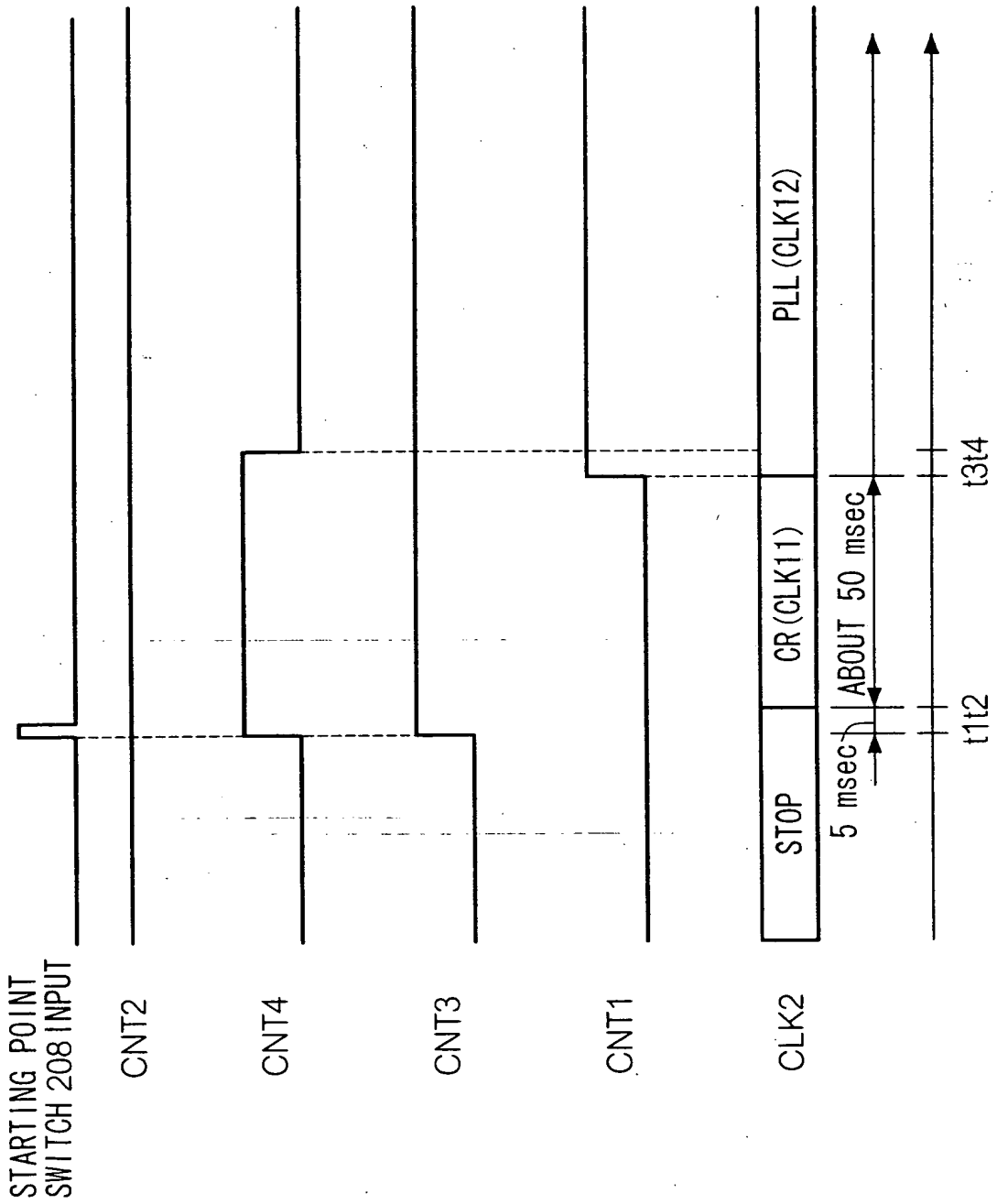

STARTING POINT SWITCH 208 INPUT
CNT2
CNT4
CNT3
CNT1
CLK2
STOP
CR (CLK11)
PLL (CLK12)
5 msec
ABOUT 50 msec
t1t2
t3t4

FIG. 15

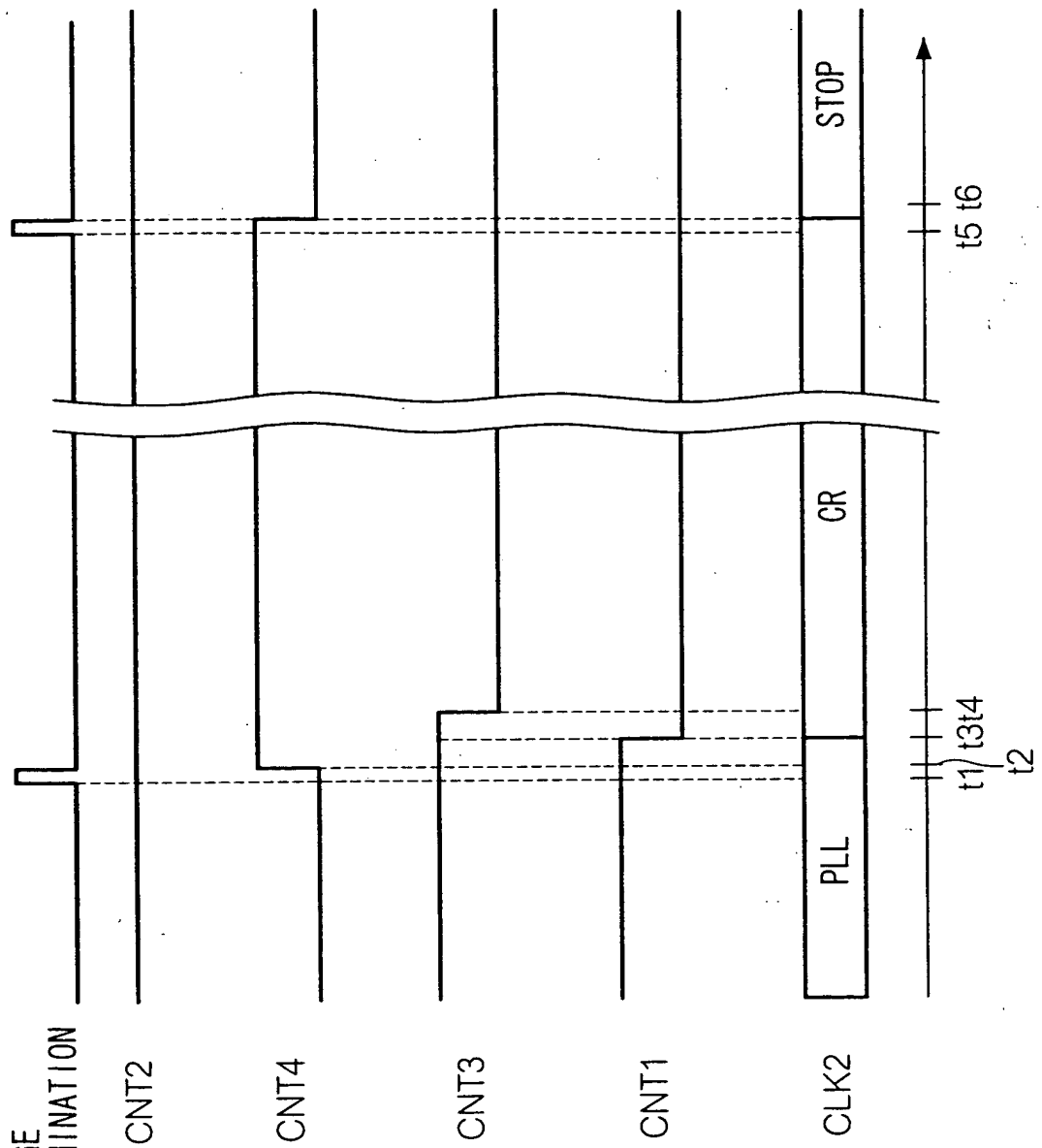

VOLTAGE DETERMINATION
CNT2
CNT4
CNT3
CNT1
CLK2
PLL
CR
STOP
t1
t3t4
t2
t5 t6

FIG. 16

FIG. 17

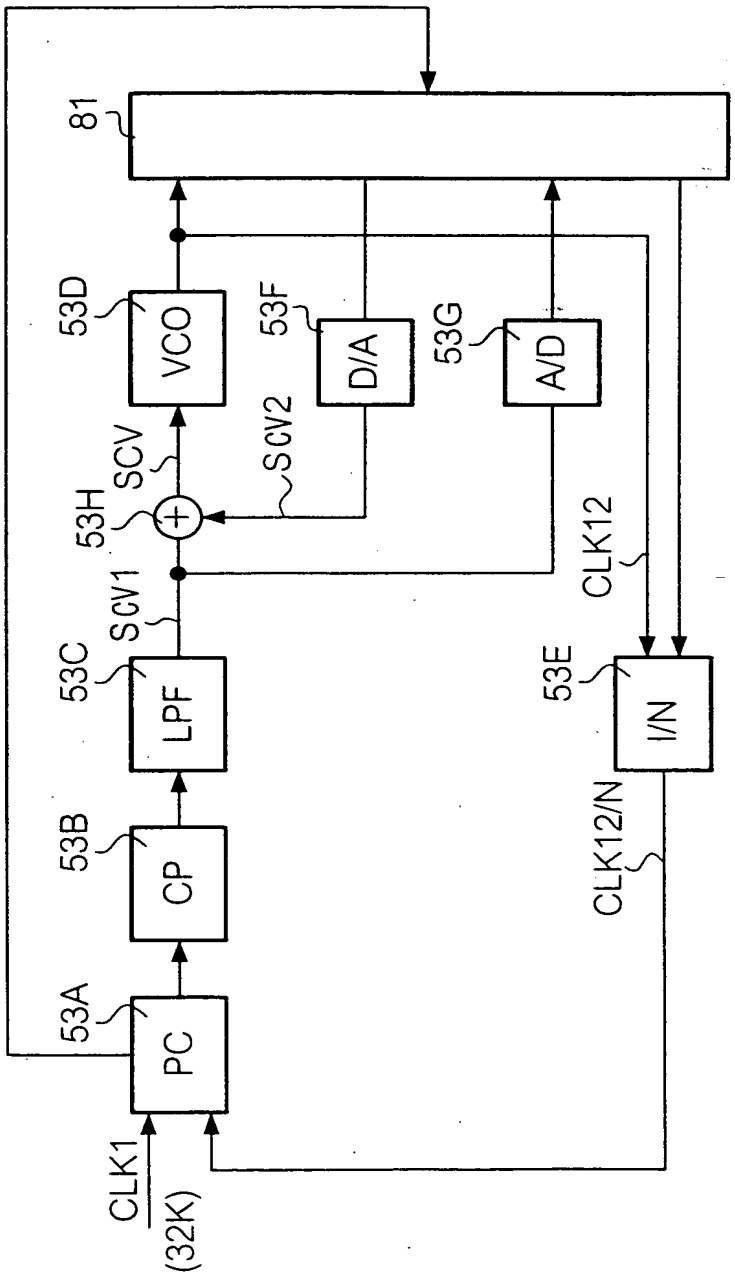

53 :PLL OSCILLATING CIRCUIT
LOCK/UNLOCK SIGNAL
81
53D
VCO
53F
D/A
53G
A/D
SCV
SCV2
53H
CLK12
SCV1
53C
LPF
53E
I/N
53B
CP
CLK12/N
53A
PC
CLK1
(32K)

FIG. 18

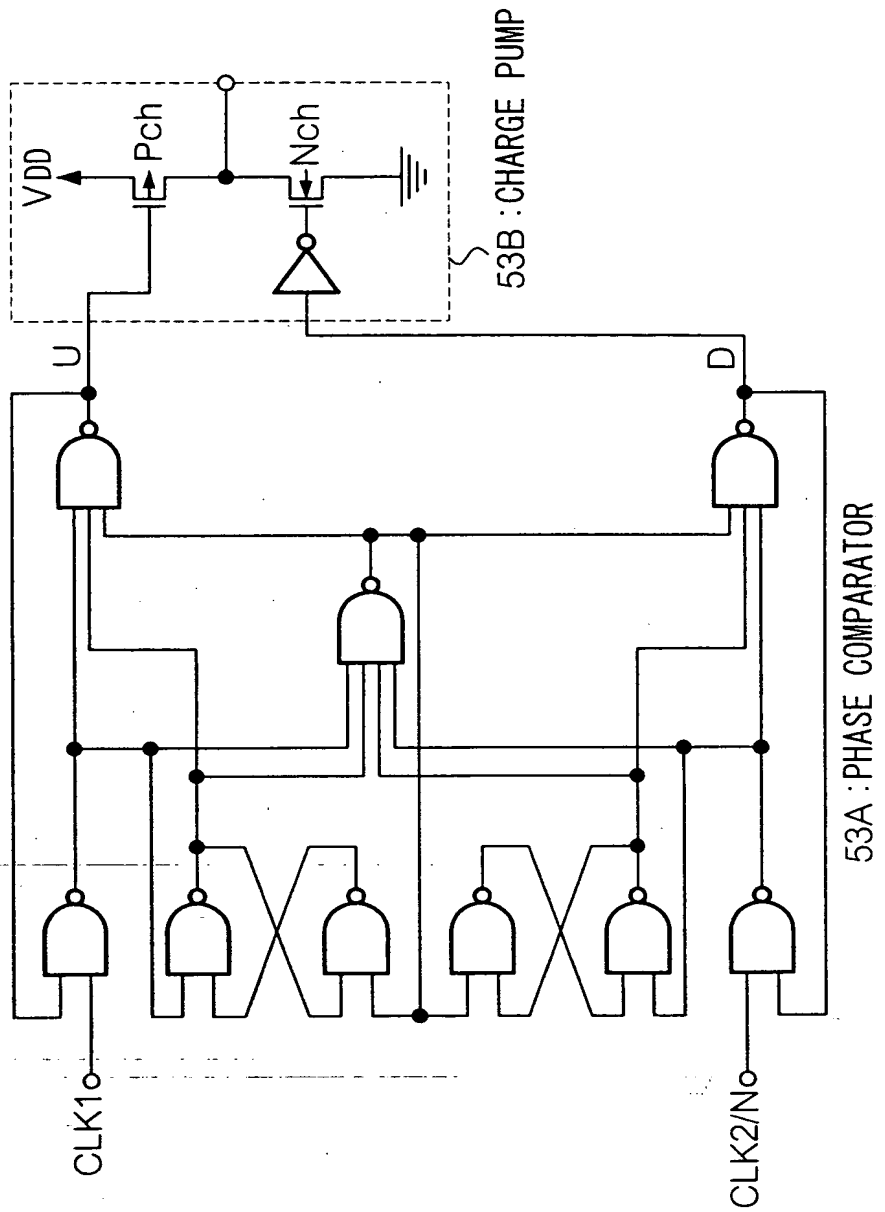

VDD
Pch
Nch
53B : CHARGE PUMP
U
D
CLK1
CLK2/No
53A : PHASE COMPARATOR

FIG. 20

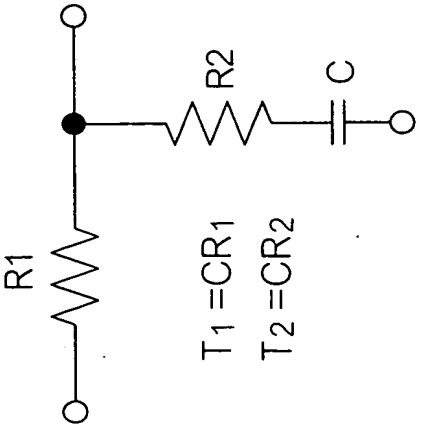

R1
R2
C
T1 =CR1
T2 =CR2

FIG. 21

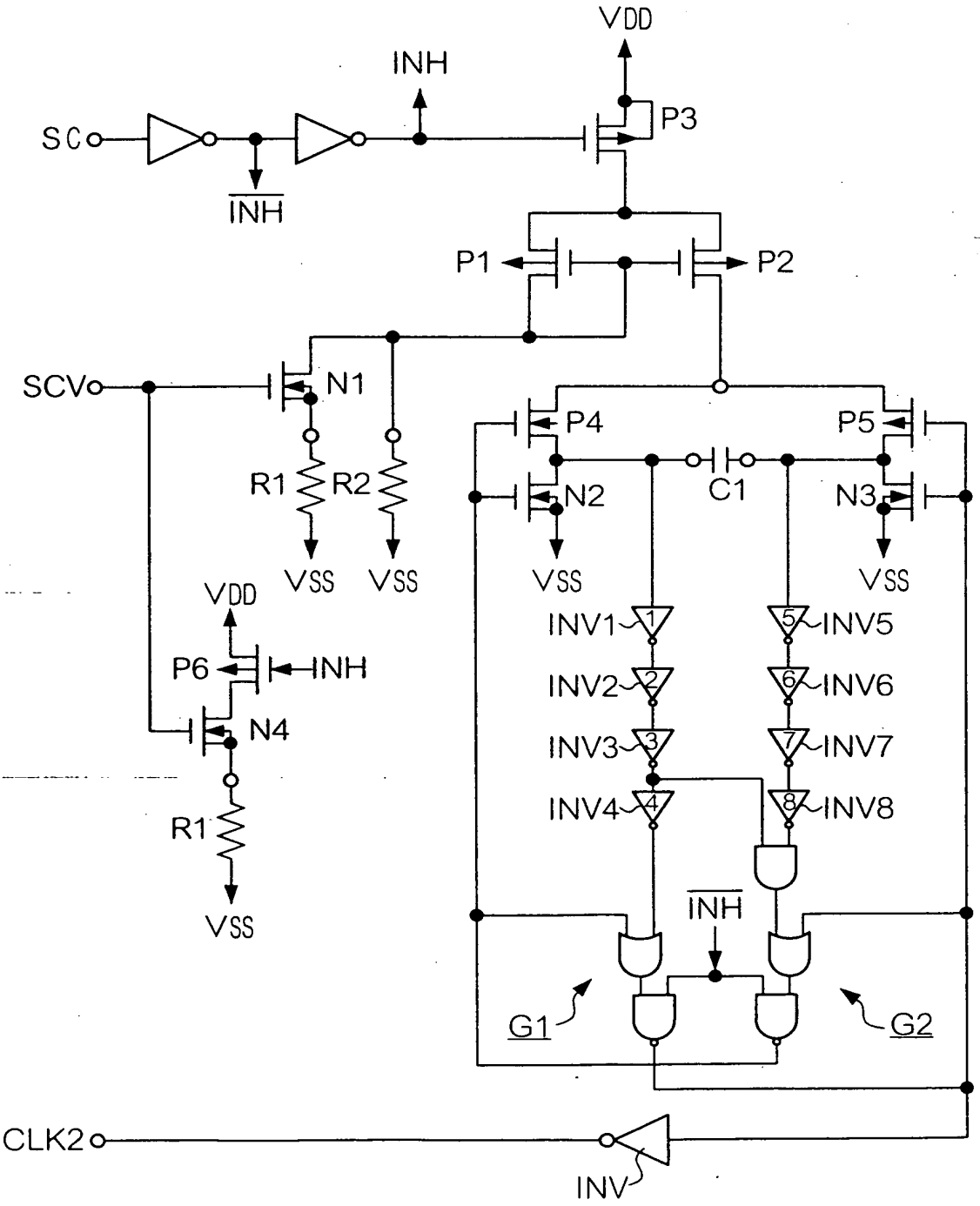

VDD
INH
SC
P3
INH
P1
P2
SCV
N1
P4
P5
R1
R2
N2
C1
N3
VSS
VSS
VSS
VSS
VDD
INV1
INV5
P6
INH
INV2
INV6
N4
INV3
INV7
INV4
INV8
R1
INH
VSS
G1
G2
CLK2
INV

FIG. 22

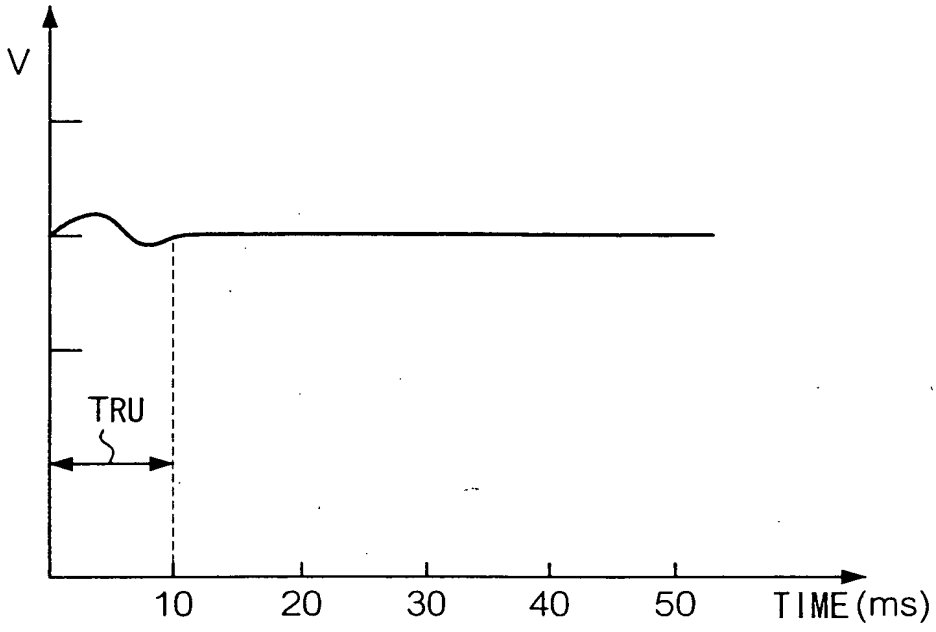

V
TRU
10
20
30
40
50
TIME(ms)

FIG. 23

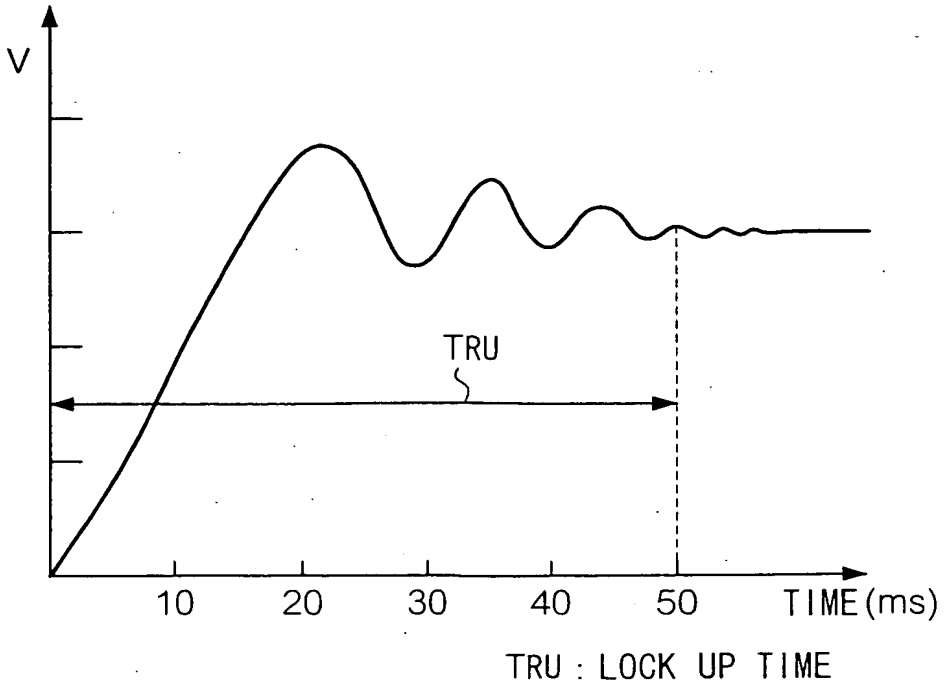
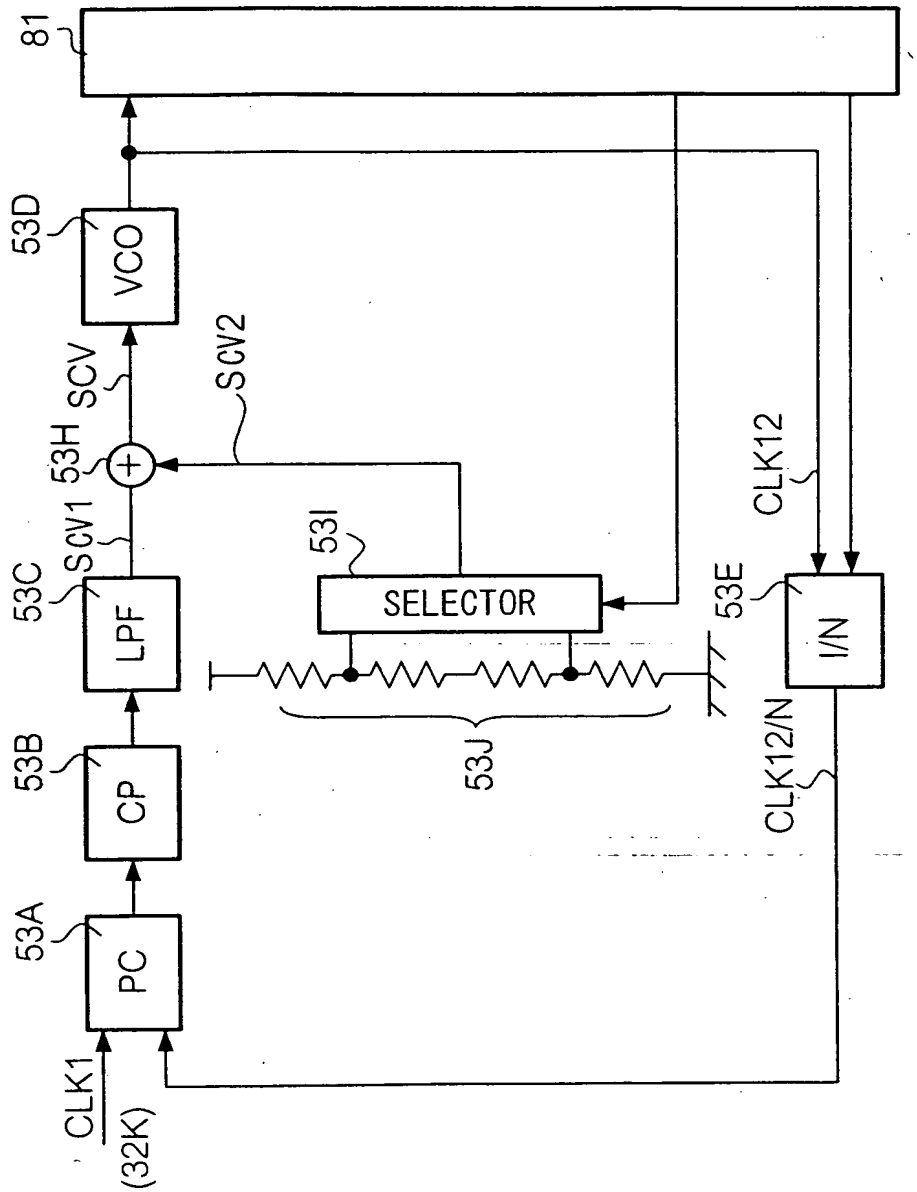

V
TRU
10
20
30
40
50
TIME(ms)
TRU : LOCK UP TIME

FIG. 24


81
53D
VCO
SCV
SCV2
53H
SCV1
53C
LPF
53I
SELECTOR
CLK12
53E
I/N
53J
53B
CP
CLK12/N
53A
PC
CLK1
(32K)